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Overview of Device SEE Susceptibility from Heavy Ions

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OVERVIEW OF DEVICE SEE SUSCEPTIBILITY FROM HEAVY IONS

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Abstract

A fifth set of heavy ion single event effects (SEE) test data have been collected since the last IEEE publications (1, 2, 3, 4) in December issues for 1985, 1987, 1989 and 1991. Trends in SEE susceptibility (including soft errors and latchup) for state-of-the-art parts are evaluated.

Introduction

Ongoing SEE test programs at JPL ,The Aerospace Corporation, the European Space Agency (ESA), CNES and other organizations are continuing to assess specific part performance for interplanetary and satellite environments and to establish SEE response trends of an ever-increasing body of device data.

In 1985, Nichols et al (Ref. 1) published the first nearly comprehensive listing of SEE test data for 186 parts. This presentation was updated in 1987 (Ref. 2) with the publication of data for 83 additional parts, in 1989 (Ref. 3) with data for 154 parts, and in 1991 (Ref. 4) with data for 182 parts. In this paper, the authors extend the data base for 165 new parts. As before, the data are collected according to technology, function and manufacturer in order to identify trends, generalizations and data gaps.

Testing Approaches

The experimental procedures, such as those used by JPL and The Aerospace Corporation, are evolutionary and are described in detail from time to time in December issues of IEEE Transactions on Nuclear Science (5,6) or in in-house reports. In general, procedures comply with the guidelines for SEE testing set forth by the ASTM F1.11 document (7). They also comply with a JEDEC 13.4 document in preparation, "Test Procedure for the Measurement of Single Event Effects in Semiconductor Devices from Heavy Ion Irradiation."

Organization and Scope of Data

This paper summarizes soft error and latchup experimental test data from the Jet Propulsion Laboratory (JPL), The Aerospace Corporation (A), John Hopkins Applied Physics Laboratory (JH), Centre National D'Etudes Spatiales (CNES, France), European Space Agency (ESA) and other SEE testers. These data are provided directly to JPL or were otherwise made available to the community during the two-year period from January, 1991, through December, 1992. We are pleased to include smaller SEE data sets generated by all U. S. and foreign researchers when these data are made directly available to us. Not included are proprietary data generated by subcontractors who used JPL hardware. Also omitted are now fairly extensive data sets on power transistor burnout obtained by JPL, Rockwell, Boeing and others-- such data require a significantly different organization.

The SEE data presented here and in the previous four reports (1,2,3, 4) represent a substantial majority of all test data obtained on SEE throughout the world. Some additional data may exist in other articles of this publication (IEEE-Nuclear Science [Dec. 1993] or this conference's IEEE Workshop Record), in other journals or in published and unpublished presentations of SEE symposia.

The data from all organizations are summarized and collected together even though there are differences in the data from each organization. For example, JPL defines the threshold LET as that value of LET where soft errors are first counted at fluences of 10^6 ions/cm^2; Aerospace now defines their LET threshold as occurring at that point where the measured upset cross section is 0.01 times the measured maximum cross section, CNES reports a threshold at 0.1 times the saturated cross section. JPL's definition virtually guarantees no upset below threshold but results in an overestimate of error rate if the cross section is erroneously assumed to be constant at all LETs greater than the threshold LET. Specifying a threshold LET at a fraction of the saturated cross section attempts to approximate the error rate better, but it introduces an arbitrary factor (to account for the slope of the

cross section vs. LET) and an assumption that the saturated value is known and/or achieved with the highest LET test ions.

The best way to calculate error rates is to use the full curve of cross section vs. LET, which may be available from the parent test organization[1], and integrate it over all angles and all ions of various LETs. But even this method, which involves the use of a computer, relies critically on what assumptions are made about grazing ion impacts and the dimensions of the device cell's sensitive volume.

All data are presently divided into two tables. Table 1 has been revised to include all SEE (soft error) data for both MOS/CMOS and bipolar devices. Table 2 exhibits data for "Latchup Tests Only". All data listed here represent a substantial abbreviation and ignore statistical features altogether. LET limits are for nominal effective values without correction for degradation that can occur when an ion traverses device overlayers. Gold data, in particular, are seldom as damaging as one would expect on the basis of nominal LET and such data are labeled when known, and Au testing is usually not recommended. SEE tests use a dynamic nominal bias (often 4.5 or 5.0 V); latchup tests are usually performed at the maximum value of the nominal bias range (e.g. 5.5V) -- a condition usually (but not always) enhancing the possibility of latchup. Reported data were taken at room temperature or ambient temperature; higher test temperature measurements may exist for some parts. In some instances, data on transients is noted, which may or may not impact electronics down the line. Hence, a system designer interested in a specific part is again urged to contact the appropriate test organization for further information.

Users are cautioned that manufacturers (Appendix I defines manufacturer abbreviations) may often change their process, and resultant SEE susceptibility, without changing the part number or notifying tester organizations. Hence, a test of flight parts is always a good policy.

Trends & Limitations

Trends and device comparisons in the recent data are offered in the "Remarks" column of Tables 1 and 2 and in the following section. However, the organized tabular format is designed to facilitate comparisons. Special studies (such as variation of SEE response with temperature) or a comparison between high energy (GANIL) heavy ion data and that from the lower energy Berkeley 88-inch cyclotron and BNL Van de Graaff are beyond the scope of this presentation. In addition, test data for the whole class of catastrophic failures of power transistors, both MOSFET and bipolar, has recently been organized by Nichols under a substantially different format.

[1] JPL data, including more recent results, may be accessed directly from JPL's computer data base, RADATA.

Some colleagues have commented that a measure of the shape of the cross sections vs. LET might be useful-- such as given by a tabulation of the Weibull parameters. Others point out that it may be more difficult to assure that such parameters are properly derived and applied than it is to calculate SEE rates directly from known (and readily available) experimental cross sections.

Program managers concerned with critical system reliability issues will ultimately need an appropriate set of cross sectional data to assess statistical features and focus on specific answers. Ballpark estimates will also have a place, however, by helping assure that expensive experiments are limited to only critical SEE issues.

An Evaluation of SEE Data

Microprocessors

JPL tested a large body of SEE data for microprocessors this year, mostly with 16-bit and 32-bit capability. Soft error thresholds are consistently low for all high-capability machines, with LET(th) ranging from approximately 1 to 10 MeV/(mg/cm^2). Important exceptions are two 16-bit devices by Marconi (GEC-Plessey), using their well-established SEE-resistant SOS technology. Most microprocessors are not very susceptible to latchup although there are exceptions (e.g. the IDT R3000 and R3000A.) The Intel CHMOSIV technology is marginally susceptible to latchup, whereas its earlier CHMOSIII technology was not. There is a very large set of data from ESA and Harris on the R3000 and R3000A RISC developed by many manufacturers.

Questions raised last year regarding the best approach to microprocessor testing remain open. The purists argue that static testing of known registers in a known state is the best approach to understanding SEE effects. JPL presently pursues this view and has demonstrated that not all elements of a microprocessor are equally SEE-susceptible. The pragmatists claim that testing with dynamic programs (the more the better) will usually show that static tests provide an unrealistic worst case.

Some data taken by European groups at GANIL, the higher-energy (10 to 100 MeV/amu) cyclotron in France, are available. The results suggest that these ions, which are more representative of interplanetary cosmic rays, are more damaging than the familiar lower-energy (2 MeV/amu) ions provided by Brookhaven's Van de Graaff and Berkeley's 88-inch cyclotron. Direct comparisons between energy regimes are few.

It will also be observed in Table 1 that there are data for several controllers and processors of various types. They have similarly low soft error thresholds [< 10 MeV/(mg/cm^2)] and varying latchup susceptibility.

Analog-to-Digital Converters (ADCs)

There are several data sets for ADCs and data for two digital-to-analog converters (DACs). Much of the data were taken by JPL in a quest for the least SEE-susceptible 12-bit ADC. The MAXIM devices were clear standouts in this subcategory, but one observes that a completely hard ADC or DAC is a rarity. This is one device type where knowledge of how the device ties in with the system is an all-important consideration in assessing its ultimate suitability.

Static RAMs (SRAMs)

There is much new data to add to the accumulation for SRAMS--with device sizes up to 4 Mbits. All devices employ variations of CMOS technology this test period, and SOI and SOS offer markedly superior resistance to soft errors and latchup. Epi technology (where the epi layer is less than ~10 microns thick) is a good guarantee against latchup but offers no significant advantages against soft errors. A tendency toward stuck bits was observed in the 0.5 micron feature-size Hitachi 4 M SRAM.

Other RAMS

ESA tested a large set of 4M DRAMs and observed a consistent very low soft error threshold typical of this device function. Some non-volatile RAMs were tested-- with two Ferroelectric RAMs (FRAMs) for the first time. Some bipolar and CMOS PROMs exhibited relatively high SEU thresholds, but one should note that PROMs are occasionally susceptible to latchup.

Gate Arrays & Bus Controllers

Several gate arrays, configured in different ways, were tested. It is difficult to sort out the large variability in soft error threshold-- even among devices made by the same manufacturer. It is encouraging that no cases of latchup were reported.

Latchup Data

Tests for latchup only are much easier to set up than those designed to measure soft errors as well. Such data are given separately in Table 2-- primarily for devices with different variations of CMOS technology. It has so far held true that bipolar devices will not latchup with heavy ions. However, latchup has occurred in bipolar devices when exposed to high intensity gamma pulses, and the requisite pnpn parasitic structure exists.

The LET thresholds listed in Table 2 are for latchup only, and cross section data is rarer because of the difficulty in obtaining repeat measurements where catastrophic burnout and overheating may occur. Also presented are data for GANIL which appears to have a devastating effect-- including latchup in several devices with epi technology. Once again a need to compare data on identical parts for both high energy GANIL ions and lower-energy ions is manifest.

JPL was able to employ Cf-252 usefully for the first time-- as a screen to reject some ADCs because of latchup. It is cautioned, however, that Cf-252 can never be used to pass a part for latchup because of the possibility that the fission ions do not have adequate range to maintain an adequate LET while generating a funnel at the well-substrate junction.

Latchup observed by MIT-Lincoln Lab in the NSC driver/receivers 26C31 & 26C32, a pair of linear devices, is explained by Sferrino [9]. He notes that the chips have tri-stated digital outputs, comprising an npn and pnp transistor in series-- the familiar structure for latchup paths. This result suggests that other transistor arrangements, such as silicon-controlled-rectifiers, may be susceptible to latchup.

Conclusions

The new data presented here can be combined with data given in References (1, 2, 3 and 4) to develop certain generalizations useful for protecting flight electronics from SEE. Hard technologies and unacceptably soft technologies can be flagged. In some instances, specific tested parts can be taken as candidates for key functions-- such as microprocessing or memory. As always with radiation test data, specific test data for qualified flight parts is recommended for critical applications. Calculations of accurate SEE rates will require the assistance of a computer code, a well-defined environment [in terms of flux vs. LET] and a complete device characterization [cross section vs. LET at the appropriate temperature.] Evaluation of catastrophic effects requires its own statistical treatment, in which flares are considered. The recent concern of JPL and others with power transistor burnout and single event gate rupture is beyond the scope of this compendium.

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Appendix I – Manufacturer Abbreviations

ACT	Actel Corp.
ADA	Advanced Analog
ADI	Analog Devices Inc.
ALS	Allied Signal
ALT	Altera Corp.
AMD	Advanced Microdevices Corp.
ATM	Atmel
ATT	American Tel & Tel
BUB	Burr-Brown Research
CRY	Crystal Semiconductor Inc.
CYP	Cypress Corp.
DAT	Datel
DDC	DDC ILC Data Device Corp.
EDI	EDI Corp.
FER	Ferranti
FUJ	Fujitsu Ltd.
GEC	GE
HAR	Harris Corp., Semiconductor Div.
HIT	Hitachi Ltd.
HON	Honeywell Inc.
IBM	IBM
IDT	Integrated Device Technologies, Inc.
INM	INMOS Corporation
INT	Intel Corp.
LDI	Logic Devices Inc.
LTC	Linear Technology Corp.
LSI	LSI Logic Corp.
MED	Marconi Electronic Devices
MCN	Micron Technologies
MIT	Mitsubishi
MMI	Monolithic Memories Inc.
MOT	Motorola Semiconductor Products Inc.
MPS	Micro Power System
MTA	Matra Harris SemiconductorMXM MAXIM
NAT	Natel Engineering
NEC	Nippon Electric Corp.
NSC	National Semiconductor Corp.
OWI	Omni-Wave, Inc.
PFS	Performance Semiconductor Corp.
PLS	Plessey Semiconductors
PMI	Precision Monolithics, Inc.
RAY	Raytheon Co., Semiconductor Divison
RCA	Radio Corporation of America
RTN	Ramtron
SAM	Samsung
SEI	Seiko
SEQ	SEEQ Technology Inc.
SGN	Signetics Corp.
SIE	Siemens Inc.
SIL	Siliconix
SIP	Sipex
SLG	Silicon General
SNL	Sandia National Laboratories
SNY	Sony Corp.
SOR	SOREP
TEL	Teledyne Crystalonics
TIX	Texas Instruments Inc.
TMS	Thomson Military & Space, France
TOS	Toshiba
TRW	TRW Inc.
UTM	United Technologies Microelectronics Center
WAF	Waferscale
XIC	Xicor Inc.
XIL	Xilinx Corp.
ZOR	Zoran
ZYR	Zyrel

Appendix II – Test Organizations

A	The Aerospace Corporation; El Segundo, CA
BPS	Boeing Physical Sciences Research Center, Seattle
CLM	Clemson University; Clemson, SC
CNES	Centre National d'Etudes Spatiales; Toulouse, France
ESA	European Space Agency-- several facilities
GD	General Dynamics
GDD	NASA Goddard Space Flight Center; Greenbelt, MD
GE	GETSCO, Philadelphia
HAR	Harris Semiconductor, Melbourne, FL
HON	Honeywell, Clearwater, FL
J	Jet Propulsion Laboratory (JPL); Pasadena, CA
JH	John Hopkins Applied Physics Laboratory; Laurel, MD
LIN	Lincoln Laboratories, M. I. T.; Cambridge, MA
MMS	Matra Marconi Space; Vélizy, France
NASA	NASA
NRL	Naval Research Laboratories, Washington D. C.
R	Rockwell International (Anaheim, CA)
SSS	S-Cubed, San Diego
TRW	TRW Space and Defense Sector (Los Angeles, CA)

Appendix III – Test Facilities

88-in.	=	88-inch cyclotron, Lawrence Berkeley Laboratory
BNL	=	Tandem Van de Graaff, Brookhaven National Laboratory, Long Island, NY
Cf-252	=	A Cf-252 fission source
ESA	=	European Space Agency-- several sites
GANIL	=	Cyclotron for Heavy Ions; Caen, France
HAR	=	Van de Graaff at Harwell, England
IPN	=	Tandem Van de Graaff, Institut de Physique Nucleaire; Orsay, France
UW	=	Tandem Van de Graaff, University of Washington, Seattle

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[9] Vince Sferrino, MIT Lincoln Lab, private communication.

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TABLE 1. SEU DATA – 1991-1992 (MOS & BIPOLAR DEVICES)

Test Org.*****	Device	Function	Technology	Mfr.*	Bits	Effective LET** Threshold	Device Cross Section (cm^2)***	Cross Section Per Bit (sq μm)	Facility****	Remarks
J	80C85RH	MicroP 8-bit	CMOS/epi	HAR	95 bits tested	30	–	65 @ LET=60	BNL	7/91. No LU>120. See also J: 6/87.
J	81C55RH	Peripheral to 8085	CMOS/epi	HAR	~2K	40	4E-3[1]	200	88-In	9/91. [1] RAM data at high LET.
CNES	SBP9989	MicroP 16-bit	Bipolar(I^2L)	TIX	–	8	1E-2	–	GANIL	11/90. Chapuis.
ESA	80C86-2/B	MicroP 16-bit	CMOS/epi	INT	–	~1	–	1000 @ LET=9	GANIL	Harboe-Sorensen IEEE NS 7/92
ESA	80C86	MicroP 16-bit	CMOS/epi Mask 1860	HAR	–	~1	–	2000 @ LET=9	GANIL	Harboe-Sorensen IEEE NS 7/92
ESA	80C86	MicroP 16-bit	CMOS/epi Mask 3584	HAR	–	~1	–	3000 @ LET=9	GANIL	Harboe-Sorensen IEEE NS 7/92
ESA	80C86	MicroP 16-bit	CMOS/epi Masks 1860 & 1750	HAR	Test data taken with low energy Harwell Tandem Van de G. gives much smaller cross sections than preceding data.					
J	M80C186	MicroP 16-bit	CHMOS III	INT	~600	9±3	–	250[1]; 450[2] [LET=61]	BNL	9/92 [1]=AX, BP, ES [2] = Relocation, SPR, DPR, TCR
GE	80C186	MicroP 16-bit	CHMOS III	INT	510 of 752	4	–	20[LET=13]	BNL	6/92. No LU with Au @ 42° angle. See preceding.
A	MG80C186	MicroP 16-bit	CMOS	INT	–	12	1E-3	–	88-In	No LU>100. 10/91
A	MD82510	UART	CMOS	INT	–	~10	–	4000	88-In.	No LU>100. 7/91
JH	1750A	MicroP 16-bit	CMOS/SOS 3-chips	PFS	all 3 chips	19	3E-4 [MMU @ LET=60]	5	BNL	92IEEE Workshop. J. Kinnison (7/92)
J	MA31750	MicroP 16-bit	CMOS/SOS	MED[1]	–	175	No upset	No upset	BNL	6/92. LU>175. [1] GEC-Plessey
ESA	MAS281	MicroP 16-bit	CMOS/SOS	MED	–	>60	No upset	No upset	GANIL	Consistent with JPL data of 5/89 2.5 μm.
JH	RTX2010RH	MicroP 16-bit	TSOS-4 process	HAR	–	150(Au)	–	–	BNL	No LU. 92IEEE Workshop (7/92)
J	80386	MicroP 32-bit	CMOS	AMD	–	>>2.5	–	–	BNL	7/91. LU(th)<<24.
J	80386	MicroP 32-bit	CHMOSIV	INT	272	3.5±1	–	100	BNL	5 & 7/91. LU=40.
GDD	80386	MicroP 32-bit	CHMOSIV	INT	–	–	–	–	BNL	7/92. LU=27. 7E-5 cm^2.
CNES	68020	MicroP 32-bit	CMOS/epi	MOT	varies	<1.7	1E-2[1]	–	IPN	92IEEE Workshop. 1=register test
CNES	68020	MicroP 32-bit	CMOS/bulk	MOT	varies	<1.7	1E-2[1]	–	IPN	92IEEE Workshop. 1=register test
HAR	R3000	MicroP 32-bit	Adv. CMOS	PFS	~1300	<3.4	1E-3	–	BNL	5/91. No LU>120. D. Vail (HAR). Table 2. VLSI MIPS RISC.
HAR	R3000	MicroP 32-bit	Adv. CMOS	SIE	~1300	6	1E-3	–	BNL	5/91. No LU>120. D. Vail (HAR). Table 2. VLSI MIPS RISC.
ESA	R3000	MicroP 32-bit	CEMOS IV	IDT	736 (23 reg)	–	–	–	BNL	LU(th)<3.3. RISC Harboe-Sorensen 92IEEE Workshop
ESA	R3000	MicroP 32-bit	CMOS	LSI	736 (23 reg)	~3	–	300	BNL	No LU>60. RISC Harboe-Sorensen. 92IEEE Workshop
ESA	R3000	MicroP 32-bit	PACE I	PFS	736 (23 reg)	~6	–	100	BNL	No LU>60. RISC Harboe-Sorensen. 92IEEE Workshop
ESA	R3000	MicroP 32-bit	Adv. CMOS	SIE	736 (23 reg)	<10	–	100	BNL	No LU>60. RISC Harboe-Sorensen. 92IEEE Workshop
ESA	R3000	MicroP 32-bit	CMOS	NEC	736 (23 reg)	<10	–	120	BNL	LU(th)=60. RISC Harboe-Sorensen. 92IEEE Workshop
ESA	R3000A	MicroP 32-bit	CEMOS V	IDT	736 (23 reg)	~6	–	>100	BNL	LU(th)=27. RISC Harboe-Sorensen. 92IEEB Workshop
ESA	R3000A	MicroP 32-bit	HCMOS	LSI	736 (23 reg)	<8	–	100	BNL	LU(th)=60. RISC Harboe-Sorensen. 92IEEE Workshop
ESA	R3000A	MicroP 32-bit	PACE II	PFS	736 (23 reg)	<6	–	120	BNL	No LU>60. RISC Harboe-Sorensen. 92IEEE Workshop
ESA	R3000A	MicroP 32-bit	Adv. CMOS	SIE	736 (23 reg)	~6	–	200	BNL	No LU>60. RISC Harboe-Sorensen. 92IEEE Workshop
CNES	L64730	DCT Proc.	CMOS	LSI	–	8	2E-3	–	GANIL	92IEEE Workshop Dufour. 7/92
BPS	87C51FB/ 87C51FC	MicroC 8-bit	CHMOS III	INT	~2300 total	~3[1% sat]	–	400[1]	88-In	8/92 This is non-hard version of 80C51. Oberg. [1]=IRAM/DRAM LU=10; 1E-3 cm^2.

* See listing of abbreviations in Appendix I.
** LET is Linear Energy Transfer = the density of ionization along an ion's path in MeV/(mg/cm^2). The cosine law for beam angle is applied where valid to obtain "effective" LET.
**** See listing of abbreviations in Appendix III.
***** See listing of abbreviations in Appendix II.
*** Unless otherwise noted, the cross section (upsets/fluence per device) is given for 240-380 MeV Kr or Br at normal incidence, having an LET=36 to 40 MeV/(mg/cm^2).

TABLE 1. (Cont'd)

Test Org.*****	Device	Function	Technology	Mfr.*	Bits	Effective LET** Threshold	Device Cross Section (cm^2)***	Cross Section Per Bit (sq μm)	Facility****	Remarks
GDD	82380	DMA Cont. 32-bit	CHMOS III	INT	900	<11	>1E-4	–	BNL	IEEE92 Workshop Record, p1.
ESA	R3010A	FP Accel. Coprocessor	CEMOS V	IDT	1024 (32 reg.)	<8	–	>100	BNL	No LU>27. Harboe-Sorensen 92IEEE Workshop
ESA	R3010A	FP Accel. Coprocessor	HCMOS	LSI	1024 (32 reg.)	~8	–	100	BNL	LU=27. Harboe-Sorensen 92IEEE Workshop
ESA	R3010A	FP Accel. Coprocessor	–	PFS	1024 (32 reg.)	<6	–	>40	BNL	No LU>27. Harboe-Sorensen 92IEEE Workshop
ESA	R3010A	FP Accel. Coprocessor	\Adv. CMOS	SIE	1024 (32 reg.)	~6	–	200	BNL	No LU>60. Harboe-Sorensen 92IEEE Workshop
GE	80387-16	Coprocessor	CHMOS IV	INT	all 640	4	–	20[LET=24]	BNL	10/92. See Table 2. LU(th)=24 to 37.
CNES	68882	FP Coproc. 32-bit	CMOS/epi	MOT	varies	3	1E-2[1]	–	IPN	92IEEE Workshop. 1=register test
CNES	68882	FP Coproc. 32-bit	CMOS	MOT	varies	3	1E-2[1]	–	IPN	92IEEE Workshop. 1-register test
MMS	TMS320C25	DSP	CMOS	TIX(Fr?)	[Ref 1] [Ref 2]	7 7	4E-4 2E-2	–	GANIL	Dufour, 92IEEE Workshop. (1)=MPY test program; (2)=RAM test. LU=31; 1E-4 cm^2.
JH	ADSP2100A	DSP	CMOS/epi commercial	ADI	–	13	5E-3	–	BNL	LU=13.5; 1E-4 cm^2.
	JH also reports that an experimental version of the above, having a different substrate, exists with No LU>120. (See J. Kinnison, IEEE NS Dec 91, p 1398). Availability not known.									
NRL	ADSP2100A	DSP	CMOS/epi 13 μm	ADI	–	7	3E-4	–	BNL	No LU>>38, but a 17 μm epi std. production part latched up easily. M. DeLaus – 1/91.
ESA	ADSP2100A	DSP	CMOS/epi 12.5 μm	ADI	531	8	–	300	IPN	LU=12; 2E-5 cm^2. Harboe-Sorensen IEEE NS Dec 92, p 441. See above.
J	HSRD1056	Resolver Dig. Conv.	Hybrid RH CMOS	NAT	16 tested	<13	5E-5	–	BNL	12/91. No LU>110.
SSS	DAC8408	8-bit DAC	CMOS	PMI	–	45	4E-5	–	BNL	1/92. No LU>89.
BPS	AD558	8-bit DAC	Bipolar (I^2L)	ADI	–	<<5	>2E-4	–	UW	2/92.
HON	PM7545	12-bit DAC	–	PMI	–	24	1.4E-4	–	BNL	10/92. DC: 9142 No LU>>37. WP-02
A	DAC8412	12-bit DAC	BICMOS	PMI	–	25	2E-4	–	88-In	No LU>100. 10/92
HON	AD9048TQ	8-bit ADC Flash	[1]	ADI	–	<<3	3.2E-4	–	BNL	LU=7;1.3E-5 cm^2. [1]=bipolar, but LU raises questions of possible CMOS also. DC: 9142 & 9222 WP-02. 10/92
A	MP7684	8-bit ADC Flash	CMOS	MPS	–	~1	1E-3	–	88-In	12/91. See Table 2: J: No LU>120. 11/92
BPS	AD7824	8-bit ADC	CMOS	ADI	–	<<5	>1E-4[LET=10]	–	UW	2/91. FI ion only.
J	AD7672B	12-bit ADC	CMOS	ADI	–	6	2E-4[8 MSB's]	–	BNL & 88-In	7 & 9/91. No LUI>175. See Table 2.
J	MX7672	12-bit ADC	BICMOS	MXM	–	20	>2E-4	–	BNL	11/92
J	MX7572	12-bit ADC	Bipolar/CMOS?	MXM	–	20	>2E-4	–	BNL	11/92
HON	HI574	12-bit ADC	CMOS	HAR	–	10	8E-5	–	BNL	No LU>>37. 10/92 DC: 9210
J	HI674ALD	12-bit ADC	DC9205	HAR	–	6	>1E-4	–	BNL	11/92 See Below. No LU>120 at 80° C. Earlier DC is latchable.
J	HI674ASD	12-bit ADC	DC9028	HAR	–	6	–	–	BNL	11/92 LU(th)=30. See above.
J	AD574A	12-bit ADC	BIMOS	ADI	–	<3	–	–	88-In	9/91. No LU>110.
J	AD674A	12-bit ADC	Bipolar (Two chip)	ADI	–	<3	–	–	88-In	9/91. No LU>110.
J	AD674B	12-bit ADC	BIMOS	ADI	–	<3	>5E-4	–	BNL	11/92. No LU>120.
J	MX674A	12-bit ADC	BICMOS	MXM	–	~3	>1E-3	–	BNL	11/92. No LU>120.
J	ADC574A	12-bit ADC	Bipolar/CMOS	BUB	–	<<40	–	–	BNL	7/91. LU LET<<40.
J	ADC674	12-bit ADC	Bipolar/CMOS	BUB	–	<<40	–	–	BNL	7/91. LU LET<<40.
J	AD7872	14-bit ADC	BICMOS	ADI	–	<1.4	1E-3	–	BNL	9/92, No LU>104
A	HS9576RH	16-bit ADC	CMOS Hybrid	SIP	–	3	5E-4	–	88-In	No LU>100. 1/92

TABLE 1. (Cont'd)

Test Org.*****	Device	Function	Technology	Mfr.*	Bits	Effective LET** Threshold	Device Cross Section (cm^2)***	Cross Section Per Bit (sq µm)	Facility****	Remarks
JH	54AC708	FIFO	CMOS/epi	NSC	64x9	21	8E-4	–	BNL	92IEEE Workshop Kinnison
JH	74AC725	FIFO	CMOS/epi	NSC	512x9	9	3E-3	–	BNL	92IEEE Workshop Kinnison. "Minilatch"
GDD	7202RE	FIFO (10 µm)	CMOS/epi	IDT	1Kx9	3.5	4.2E-3	46	BNL	LU=38. 9/92. Compare Table 2
CLM	HC5517A	SRAM	CMOS	TIX	2Kx8	5	5E-6 @ LET=24	–	BNL	McNulty- IEEE '91
A	L6116	SRAM	CMOS/NMOS	LDI	2Kx8	5	8E-3	50	88-In	LU=15; 1E-3 cm^2. 12/92
A	CYPC128A	SRAM	CMOS/NMOS	CYP	2Kx8	2	7E-3	40	88-In	LU=10; 1E-4 cm^2. 12/92
HON	HC6116	SRAM	CMOS[1]	HON	2Kx8	14	–	100	BNL	IEEE NS 6/92 p450 [1]=with variable R.
HON	HC6216	SRAM	CMOS[1]	HON	2Kx8	25 to 40	–	80	BNL	IEEE NS 6/92 p450 [1]=with variable R.
J	HX6364	SRAM	CMOS/SOI DC9029	HON	8Kx8	>90	–	–	BNL	5/91. No LU>90 up to 125 deg C.
HON	HC6364	SRAM	CMOS/epi	HON	8Kx8	56	–	–	BNL	DC=? See above.
HAR	TS054	SRAM	Std Cell [1]	HAR	64K	>138	–	–	BNL	No LU. W. Newman 10/91. [1]=Rad Hard CMOS/SOS
ESA	MA6167	SRAM	CMOS/SOS	MED	16Kx1	~40	–	2 @ LET=75	88-In	3.0 µm technology
ESA	MA6116	SRAM	CMOS/SOS	MED	2Kx8	30	–	5 @ LET=75	88-In	3.0 µm technology
ESA	MA9187	SRAM	CMOS/SOS	MED	64Kx1	~60	–	2 @ LET=120	88-In	1.5 µm technology
J	IBM6401	SRAM	CMOS/epi	IBM	64Kx1	>115	No upset	No upset	BNL	6/92. Development SRAM. No LU>115.
ESA	EDH8832C	SRAM	NMOS/CMOS	EDI	32Kx8	~2	–	100	IPN	1/91. No LU reported IEEE 91. Compare '87. Aerospace data.
A	MT5C256	SRAM	CMOS/NMOS	MCN	256Kx1	~3	~1[1]	–	88-In	[1]=Factor of 100 lower for high R. No LU>100. 6/92
A	MT5C2568	SRAM	CMOS/epi	MCN	32Kx8	3	0.9	–	88-In	No LU>100. 7/91
MMS	MT5C2568C	SRAM	CMOS 2M-2P	MCN	32Kx8	<1	0.6	–	GANIL	LU(th)=23; 1E-2 cm^2 Dufour, 92IEE Workshop 7/92 Multiple upsets
CNES	MT5C1001	SRAM	CMOS	MCN	1Mx1	4.5	0.5	–	IPN	Date Code 9133
CNES	MT5C1008	SRAM	CMOS/epi	MCN	128Kx8	~2	0.6[1]	–	IPN	<5/91. DC8116 No LU>26. Possible multiple errors/strike. (1)=Worst case all 1's
CNES	MT5C1008	SRAM	CMOS	MCN	128Kx8	6[1]	1.8	–	IPN	Date Code 9125. [1]=at 10% of sat. See Table 2.
CNES	MT5C1008	SRAM	CMOS/epi	MCN	128Kx8	5[2]	2.0	–	IPN	Date Code 9101 (1)= Worst case all 1's [2]=at 10% of sat.
CNES	MT5C1008	SRAM	CMOS	MCN	128Kx8	<7[2]	2E-3	–	IPN	(1)=low current resistor process. [2]=at 10% of sat.
A	MT5C1008	SRAM	CMOS/epi NMOS	MCN	128Kx8	4	2	–	88-In	IEEE91. No LU>100. Multiple errors/strike. A high resistivity DUT: SEU cross=~1E-2 cm^2.
J	MT5C1008C	SRAM	CMOS/epi [new version]	MCN	128Kx8	<3	2E-2	–	88-In	9/91. No LU>110. No date code.
CNES	HMS65641	SRAM	CMOS/epi [12 µm]	MTA	8Kx8	2.5; 10[1]	0.2	300	IPN	8/91. LU=50; 4E-4 cm^2. [1]=at 10% of sat. Compare earlier CNES data.
CNES	HM65656	SRAM	SCMOS	MTA	32Kx8	6[10% sat]	0.1	–	IPN	1992. Engr. sample
CNES	HM65664	SRAM	SCMOS Final process	MTA	8Kx8	9[10% sat]	0.4	–	IPN	9/91. No LU>50. R. Ecoffet
NASA	HM1-65664	SRAM	SCMOS/epi	MTA	8Kx8	5	–	30	BNL; GANIL/IPN	12/90. 1µm.; No LU at LET=116
CNES	HM65641	SRAM	CMOS/epi	MTA	8Kx8	10	0.2	–	IPN	Date Code 8933
CNES	TS4H6408	SRAM	SOI	TMS	8Kx8	>114	–	–	IPN	Date Code 9151
A	IDT7052	SRAM	CMOS(V)/NMOS	IDT	2Kx8	4	8E-2	–	88-In	No LU>100. 10/92
A	IDT7164	SRAM	CMOS(V)/NMOS	IDT	8Kx8	3	0.1	–	88-In	LU=8; 8E-3 cm^2. 10/92
A	MCM6226	SRAM	CMOS/NMOS	MOT	128Kx8	<3	0.2	–	88-In	LU=45; 2E-5 cm^2. 10/92
A	CXK581000P-10L	SRAM	CMOS/NMOS	SNY	128Kx8	3	8E-2	–	88-In	LU=55; 2E-5 cm^2. 2/90 (Corrected)

TABLE 1. (Cont'd)

Test Org.*****	Device	Function	Technology	Mfr.*	Bits	Effective LET** Threshold	Device Cross Section (cm^2)***	Cross Section Per Bit (sq µm)	Facility****	Remarks
A	CXK581001	SRAM	CMOS/NMOS	SNY	128Kx8	3	0.15	–	88-In	LU=30; 5E-5 cm^2. 10/92
GDD	HM628512	SRAM	HI-CMOS/epi 0.5 µm feature	HIT	512Kx8	~1.5	1.25	30	BNL	9/92. No LU>90 Stuck bits seen.
R	EDI 41024C100QB Mosaic	DRAM	–	EDI	1Mx1	1.4	0.11	10	BNL	No LU>82. 4/92
R	MDM1100TMB	DRAM	–	NEC	1Mx1	<0.5	0.24	24	BNL	LU(th)=25; 1E-4 cm^2 dynamic test. 4/92
R	Mosaic MDM1400G	DRAM	–	HIT	4Mx1	~2	–	12	BNL	No LU>82. 4/92
ESA	MB814100-10PSZ	DRAM	CMOS	FUJ	4Mx1	~1	–	80	IPN	No LU>50 RADECS91
ESA	HM514100ZP8	DRAM	CMOS	HIT	4Mx1	~2	–	12	IPN	No LU>40 RADECS91
ESA	MT4C1004C	DRAM	CMOS[1]	MCN	4Mx1	~2	–	30	IPN	No LU>40 RADECS91 [1]=Engr. sample. See also Table 2 & below.
A	MT4C4001	DRAM	CMOS/epi 7 micron	MCN	1Mx4	~3	~2(4.5V)	–	88-In	No LU>100. 3/92
ESA	D424100V-80	DRAM	CMOS	NEC	4Mx1	~1	–	40	IPN	No LU>50 RADECS91
ESA	KM41C4000Z-8	DRAM	CMOS	SAM	4Mx1	~2	–	40	IPN	No LU>40 RADECS91
ESA	HYB514100J-10	DRAM	CMOS	SIE	4Mx1	~1	–	60	IPN	No LU>40 RADECS91
ESA	TMS44100DM-80	DRAM	CMOS [EPIC]	TMS	4Mx1	~1	–	40	IPN	No LU>40 RADECS91
ESA	TC514100Z-10	DRAM	CMOS	TOS	4Mx1	~1	–	60	IPN	No LU>40 RADECS91
CNES	P10C68	RAM Non-vol.	CMOS/SNOS	PLS	8Kx8	7$^{(1)}$	0.35$^{(1)}$	–	IPN	(1) = SRAM configuration.
CNES	P10C68	RAM Non-vol.	CMOS/SNOS	PLS	8Kx8	>114$^{(1)}$	–	–	IPN	(1) = EEPROM configuration.
J	FMx1408	FRAM	CMOS	RTN	2Kx8	<<30	2E-4(dyn.)	–	Cf-252	6/92. LU LET<<30
J	FMx1208	FRAM	CMOS/epi	RTN	512x8	~11	3E-3[dyn.]	–	BNL	6/92. LU LET=45.
CNES	28HC256	EEPROM	CMOS/FG	SEQ	32Kx8	>54	–	–	IPN	Date Code 9025
CNES	28HC256	EEPROM	CMOS/FG	ATM	32Kx8	>54	–	–	IPN	Date Code 9032
CNES	X28C256	EEPROM	CMOS/FG	XIC	32Kx8	–	–	–	IPN	DC 9032. Table 2
A	DM28C256	EEPROM	CMOS/epi	SEQ	32Kx8	~15* 5**	1E-4* 4E-4**	–	88-In	No LU>100. 5/91 *=READ. **=WRITE Compare following.
GDD	28C256	EEPROM	CMOS/epi	SEQ	32Kx8	3.4(write)	5E-3	–	BNL	Perm. fail @ LET=60 IEEE92 Workshop p1
MMS	CY7C261-55	EEPROM	CMOS/FG	CYP	8Kx8	<32	0.2	–	GANIL	92IEEE Workshop Dufour 7/92
MMS	WSF57C49B	EEPROM	CMOS/FG	WAF	8Kx8	45	5E-2	–	GANIL	92IEEE Workshop Dufour 7/92 LU(th)<32; 3E-4 cm^2.
MMS	HM6617	PROM	CMOS	HAR	2Kx8	32	3E-4	–	GANIL	LU=58; 2E-4 cm^2. 92 IEEE Workshop Dufour. 7/92. Compare earlier data.
MMS	R29793DM	PROM	Bipolar	RAY	8Kx8	8	3E-5 (peripherals only)	–	GANIL	No LU>87. Dufour 92IEEE Workshop
GDD	82HS641A	PROM	Bipolar	SGN	8Kx8	>73	–	–	BNL	No LU>73. 7/92. Compare to next.
MMS	82HS641	PROM	Bipolar	SGN	8Kx8	31	7E-6	–	GANIL	No LU>120 7/92 Compare above.
J	UT1553	Bus Controller	CMOS/epi	UTM	164/732	60	–	–	BNL	5/91. No LU>120.
MMS	TC02	MACS Bus Cont.	MA GA	MTA	–	110	>3E-6	–	GANIL	No LU>124. Dufour 92IEEE Workshop
GDD	Bus Cont.	ASIC (Bus)	CMOS/epi	MTA	–	8	1.5E-5	–	BNL	No LU>87. 7/92 FSC design
GDD	Serial Cont.	ASIC (Bus)	CMOS/epi	MTA	–	4.5	>4E-5	–	BNL	No LU>87. 7/92 FSC design

TABLE 1. (Cont'd)

Test Org.*****	Device	Function	Technology	Mfr.*	Bits	Effective LET** Threshold	Device Cross Section (cm^2)***	Cross Section Per Bit (sq µm)	Facility****	Remarks
CNES	ULA 5N104	ASIC (Bus)	Bipolar	FER	–	<5.5	2E-3	–	GANIL	Chapuis, ESA Conf. 11/90 No LU>88.
MMS	MC5000	Gate Array (Memory Plan.)	CMOS	MTA	–	30	5E-3	–	GANIL	No LU>62. Dufour 92IEEE Workshop See JPL data '87.
HON	HR1060	Gate Array	RICMOS III	HON	Multicell	22	–	1200[1]	88-In	7/91 [1]=D flip-flop [2]=RAM config.
GDD	XC3090	FPGA	CMOS	XIL	–	–	–	–	BNL	LU(th)=5; 5E-3 cm^2 DC9110 & 9045. 7/92
A	A1280	FPGA	CMOS/epi (1.2 µm feature)	ACT	1200	30[1] 5[2]	–	300[1] 8000[2]	88-In	1991, ACT II family [1]=C module [~10 PLD-equivalent gates.] [2]=S module. No LU>120. See Ref. 8
A	LRH10038Q	PPGA[1]	CMOS/epi rad-hard (1.5 µm feature)	LSI	38K gates	30	–	10	88-In	See Ref. 8 [1]=Process Prog. G A No LU>120.
A	HP03	PPGA	CMOS/epi rad-hard (1.5 µm feature)	UTM	Test Chip	45	–	10	88-In	See Ref. 8 No LU>80.
A	RA20K	PPGA	CMOS/epi rad-hard (1.0 µm feature)	UTM	Test Chip	55	–	100	88-In	See Ref. 8 No LU>120. 3/92 D F/F's; SRAM
ESA	EP310	Prog. Logic Dev.	–	ALT	–	5.4	3.6E-6(sat)	–	HAR[1]	6/91 [1]=Van de G.
ESA	EP600	PLD	–	ALT	–	8	3E-6(sat)	–	HAR[1]	6/91 [1]=Van de G.
ESA	20RA10Z	PLD	–	SEQ	–	–	4.2E-5	–	Cf-252	6/91. Latchup.
GDD	22V10C-10	PAL	BICMOS	CYP	–	>120	–	–	BNL	No LU>120. 12/92
GDD	22V10D-15DMB	PAL	CMOS	CYP	–	–	–	–	BNL	LU(th)<<26. 12/92
A	22V10B	PAL	CMOS	CYP	–	5	–	–	88-In	LU(th)=12; 5E-4 12/92
IBM	22V10	PAL	CMOS	CYP	–	5	7E-6	–	BNL	LU(th)=25; 3E-4 cm^2 Die similar to below.
IBM	22V10	PAL	CMOS	MMI	–	5	1E-5	–	BNL	LU(th)=25; 3E-4 cm^2 Die similar to above.
A	22V10A	PAL	Bipolar	AMD	–	4	2E-5	–	88-In	6/92
A	22V10A	PAL	Bipolar	TIX	–	4	2E-5	–	88-In	6/92
IBM	IDT49C460	EDAC (32-bit)	CMOS	IDT	–	17	–	–	BNL	LU(th)=25; 2E-3 cm^2.
A	IDT49C460	EDAC (32-bit)	CMOS	IDT	–	>100	<1E-7	–	BNL	No LU>100. 5/91 Compare preceding.
IBM	–	EDAC (32-bit)	CMOS	AMD	–	5	1E-4	–	BNL	LU(th)=25; 5E-4 cm^2.
MMS	54LS630	EDAC	LSTTL	TIX	–	7	1E-3	–	GANIL	No LU>32. Dufour, 92 IEEE Workshop
MMS	54LS74A	D- FF	LSTTL	TIX	4	7	1E-4	2500	GANIL	No LU>32. Dufour, 92 IEEE Workshop
MMS	MC10531	D- FF	bipolar/ECL	MOT	4	<32	1E-5	250	GANIL	No LU>116. Dufour, 92 IEEE Workshop
A	54LS112	J-K/FF	TTL(LS)	MOT	2	6	1E-4	5000	88-In	6/92
BPS	555	Timer	bipolar	NSC	–	5	>2E-5(LET=10)	–	UW	2/92
BPS	555	Timer	bipolar	SGN	–	5	>2E-5(LET=10)	–	UW	2/92
MMS	54ACT163	Counter	FACT	MOT	–	80	6E-6	–	GANIL	No LU>140. Dufour, 92 IEEE Workshop
MMS	54ACT374	D FF	FACT	MOT	–	>140	–	–	GANIL	No LU>140. Dufour, 92 IEEE Workshop
HON	54ACTQ373	D-Latch	–	NSC	Octal	29	8.6E-5	–	BNL	No LU>>37. DC8942 Wp-02 10/92
A	54HCT373	Latch	CMOS/HCT	TIX	Octal	~70	5E-6	–	88-In	No LU>100. 1/91
A	54HCT393	Counter	CMOS/HCT	HAR/GE	8	23	4E-5	–	88-In	No LU>100. 6/92
J	PWM1526	PWM	bipolar (&1 JFET)	SLG	–	10	2E-3	–	88-In	9/91. No LU>110.

TABLE 2. LATCHUP TEST ONLY (1991-1992)

Test Org.*****	Device	Function	Technology	Mfr.*	Bits	Effective LET** Threshold	Device Cross Section (cm^2)***	Facility****	Remarks
JH	64500/1	MicroP (16-bit)	CMOS/epi	LSI	–	75	–	BNL	1750A CPU.
LIN	68020	MicroP (16-bit)	CMOS/epi	MOT	–	32±6	–	BNL	4/91
A	HS82C88	Bus Cont.	CMOS	HAR	–	55	4E-6	88-In	12/91
A	HS82C59A	Priority Int. Controller	CMOS	HAR	–	16	2E-3	88-In	12/91
A	HS82C52	Ser. Cont. Interface	CMOS	HAR	–	50	2E-5	88-In	12/91
HAR	R3000	MicroP (32-bit)	CMOS?	IDT	–	4.8	–	BNL	May 91. Table 1. MIPS RISC. D. Vail (HAR)
HAR	R3000A	MicroP (32-bit)	CMOS?	IDT	–	26	–	BNL	May 91. Table 1. MIPS RISC. D. Vail (HAR)
HAR	R3000A	MicroP (32-bit)	CMOS?	PFS	–	60	–	BNL	May 91. Table 1. MIPS RISC. D. Vail.
HAR	R3000	MicroP (32-bit)	CMOS	LSI	–	53	–	BNL	May 91. Table 1. MIPS RISC. D. Vail.
MMS	L64801	MicroP (32-bit)	CMOS/epi	LSI	–	16.5	4E-3	GANIL	SPARC. Dufour, 92 IEEE Workshop
MMS	L64811	MicroP (32-bit)	CMOS	LSI	–	8.2	5E-2	GANIL	SPARC. Dufour, 92 IEEE Workshop
MMS	L64814	F.P.U. (32-bit)	CMOS/epi	LSI	–	10	2E-3	GANIL	SPARC. Dufour, 92 IEEE Workshop
MMS	T800	Transputer (32-bit)	CMOS	INM	–	45	>1E-4	GANIL	Dufour, 92 IEEE Workshop
A	WE-DSP32C	DSP	CMOS	ATT	–	17	1.7E-2	88-In	June 1992
J	320C25	DSP	CMOS/epi	TIX (France)	–	36 @ 1E5 ions/cm^2	–	BNL	LU=26 at 125 deg. C 5/91. DC 8939. Compare to earlier data. See Table 1.
JH	320C25	DSP 6 μm epi	New CMOS/epi	TIX	–	80	–	BNL	92 IEEE Workshop, Kinnison. 7/92. See previous & Table 1.
A	320C30	DSP	CMOS/epi 7 μm	TIX	–	13	5E-5	88-In	12/92. Compare to IEEE 91
J	320C50	DSP	CMOS/epi	TIX	–	>69	–	BNL	6/92
LIN	56001	DSP	CMOS	MOT	–	12	–	BNL	4/91. Dynamic test. See also Table 1.
JH	ADSP2100A	DSP (16-bit)	CMOS/epi 18 μm	ADI	–	13	1E-4	BNL	IEEE NS (Dec 91) p 1398. See below.
MMS	ADSP2100A	DSP (16-bit)	CMOS/epi	ADI	–	26	1E-3	GANIL	92 IEEE Workshop Dufour 7/92
JH	ADSP2100	DSP (16-bit)	–	HIT	–	9±2	–	BNL	4/90
MMS	ADSP2100	DSP (16-bit)	CMOS/epi	ADI	–	<30	–	GANIL	92 IEEE Workshop Dufour 7/92
J	AM29CEPL154	MicroC.	CMOS	AMD	–	10	2E-3	BNL	6/92
CNES	68881	Coprocessor	HCMOS/bulk 1.5 μm	MOT	Custom	6	4E-3	IPN	DC 8942 Compare to 68882 below.
CNES	68882	Coprocessor	HCMOS/bulk 1.2 μm	MOT	Custom	12	1E-3	IPN	DC 9022. compare to 68881 above.
J	80387	Coprocessor	CHMOS IV	INT	all 640	40	3E-5*(sat)	88-In	9/91. *Deduced from INT 80386 -- Table 1, CHMOS IV (J; 7/91).
GE	80387-16	Coprocessor	CHMOS IV	INT	all 640	24 to 37	–	BNL	10/92. See Table 1.
GDD	80387	Coprocessor	CHMOS IV	INT	all 640	31	4E-5(sat)	BNL	7/92
J	MP7684/MP7684A	8-bit ADC (Flash)	CMOS	MPS	–	>120	–	BNL	11/92. Up to 125°C.
CNES	TMS8338	8-bit ADC	CMOS (HS13)	TMS	–	~20	5E-4	IPN	Aug 91 See following entry.
CNES	TMS8338	8-bit ADC	CMOS (HCMOS3)	TMS	–	12	2E-3	IPN	Aug 91 See preceding entry.
A	MP7695	10-bit ADC	CMOS	MPS	–	>>100	–	88-In	Jun 92
TRW	ADC87	12-bit ADC	Hybrid? DC: 8920/9128	BUB	–	? [LET=60]	>>3E-5	BNL	7/92. T.C. Lunn
TRW	ADC85	12-bit ADC	Hybrid? DC: 9203	SIP	–	>>60	–	BNL	7/92. T.C. Lunn
J	SP7800	12-bit ADC	CMOS	SIP	–	<<30	<1E-4	Cf-252	4/92
J	LTC1272	12-bit ADC	CMOS	LTC	–	<<30	–	Cf-252	10/92
J	HI774B	12-bit ADC	BICMOS	HAR	–	<<30	–	Cf-252	10/92 (DC9022)
								BNL	11/92

* See listing of abbreviations in Appendix I.

** LET is Linear Energy Transfer = the density of ionization along an ion's path in MeV/(mg/cm^2). The cosine law for beam angle is applied where valid to obtain "effective" LET.

**** See listing of abbreviations in Appendix III.

***** See listing of abbreviations in Appendix II.

*** Unless otherwise noted, the cross section (upsets/fluence per device) is given for 240-380 MeV Kr or Br at normal incidence, having an LET=36 to 40 MeV/(mg/cm^2).

TABLE 2. (Cont'd)

Test Org.*****	Device	Function	Technology	Mfr.*	Bits	Effective LET** Threshold	Device Cross Section (cm²)***	Facility****	Remarks
LIN	ADS112	12-bit ADC	–	DAT	–	38	–	BNL	4/91
SSS	CS5016	16-bit ADC	CMOS	CRY	–	<<12	–	BNL	1/92. Compare JH; Aerospace data [5/90].
A	CS5016	16-bit ADC	CMOS/epi	CRY	–	15	5E-3	88-In	5/91. See above.
J	AD7533	10-bit DAC	CMOS	ADI	–	>120	–	BNL	11/92. Up to 125 °C.
J	MP7533	10-bit DAC	CMOS	MPS	–	>120	–	BNL	11/92. Up to 125 °C.
MMS	SOR7541	12-bit DAC	CMOS	SOR	–	>116	–	GANIL	Dufour, 92 IEEE Workshop
JH	7134RT	FIFO	CMOS	IDT	8Kx8?	15	–	BNL	Kinnison 4/92
JH	7202RT	FIFO	CMOS	IDT	1Kx9?	15	–	BNL	Kinnison 4/92
GDD	7202RE	FIFO	CMOS/epi	IDT	1Kx9	38	–	BNL	See Table 1.
MSS	M67202	FIFO	SCMOS/epi RT	MTA	1Kx9	>140	–	GANIL	92 IEEE Workshop Dufour 7/92
GD	CYC185	SRAM	CMOS	CYP	8Kx8	<<40	8E-5	Cf-252	4/94 SEE Symp. High Temp data exists.
CNES	HM65641	SRAM	CMOS/epi	MTA	8Kx8	<55	–	IPN	Chapuis, at ESA Conf. 11/90
MMS	HM65664	SRAM	SCMOS/epi RT	MTA	8Kx8	>140	–	GANIL	92 IEEE Workshop Dufour 7/92. See Table 1.
MMS	HM65656	SRAM	SCMOS/epi RT	MTA	32Kx8	>140	–	GANIL	92 IEEE Workshop Dufour 7/92. See Table 1.
ESA	D4464D	SRAM	CMOS	NEC	64K	~2	0.15[LET=12]	Harwell	IEEE '92. Proton LU also occurs.
LIN	MT5C1608	SRAM	–	MCN	2Kx8	27	–	BNL	April '91
LIN	MT5C2568	SRAM	CMOS/epi	MCN	32Kx8	>164	–	BNL	Sferrino '91
LIN	MT5C2568	SRAM	CMOS	MCN	32Kx8	38 to 69	–	BNL	Sferrino '91 Compare above.
MS	MT5C1008CW	SRAM	CMOS/bulk	MCN	128Kx8	75	4E-4	GANIL	Compare Table 1. 92 IEEE Workshop Dufour, 7/92
LIN	DPS92256G	SRAM	CMOS	HIT	32Kx8	<27	–	BNL	Sferrino '91
CNES	MT4C1004C	DRAM	CMOS/epi 0.8 μm epi	MCN	1Mx4	>54	–	IPN	DC 9109
LIN	R29793	SROM	CMOS/epi? fuse-link	RAY	8Kx8	>164	–	BNL	Sferrino '91
CNES	X28C256	EEPROM	CMOS/FG	XIC	32Kx8	18	1E-3	IPN	Date Code 9032
LIN	28C256	EEPROM	CMOS/epi	SEQ	32Kx8	>164	–	BNL	Sferrino '91
LIN	28C64	EEPROM	CMOS/epi?	SEQ	8Kx8	>164	–	BNL	Sferrino '91
MMS	MB7144E	PROM	Bipolar	FUJ	8Kx8	>104	–	GANIL	92 IEEE Workshop Dufour 7/92
CNES	1020A	FPGA	CMOS/epi	TIX[1]	–	>27	–	IPN	DC 9109 [1] = 547 logic modules, 4 ports/module, config. antifuse
MMS	MC5000	GA 35K	SCMOS/epi RT	MTA	–	>80	–	GANIL	92 IEEE Workshop Dufour 7/92
MMS	MA805	1553 Bus Cont.	CMOS	MED	–	<36	–	GANIL	92 IEEE Workshop Dufour 7/92
MMS	TMC2210	Mult./Accum.	CMOS	TRW	–	>61	–	GANIL	92 IEEE Workshop Dufour 7/92
A	ATW28XX	DC/DC Conv. module (one IC)	CMOS	ADA	–	51 to 80	1E-6	88-In	10/92
J	26C31	Driver	CMOS/SOS	HAR	None	>120	–	BNL	9/92
LIN	26C31	Driver	CMOS	NSC	None	20	–	BNL	Sferrino '91
J	26C32	Receiver	CMOS/SOS	HAR	None	>120	–	BNL	9/92, saturated SEU=3E-5 cm^2
LIN/SSS	26C32	Receiver	CMOS	NSC	None	20	–	BNL	LIN: 1991; S^2: 1992
A	LTC485CN8	Transceiver	CMOS	LTC	–	3	8E-5	88-In	June 1991
MMS	DG271	Analog Switch	CMOS	SIL	Quad	>137	–	GANIL	92 IEEE Workshop Dufour 7/92
MMS	DG300	Analog Switch	CMOS	SIL	Dual	>137	–	GANIL	92 IEEE Workshop Dufour 7/92
A	DG601AK	Analog Switch	CMOS/epi 13 microns	SIL	–	>100	–	88-In	3/92
A	IH6208	Analog MUX	CMOS	HAR	–	>100	–	88-In	12/92
A	LTC1064	Low Pass Filter	CMOS	LTC	–	15	3E-4	88-In	12/92
JH	54ACTQ244	Logic	FACT w. I/O	NSC	–	>120	–	BNL	1/91 -- NSC's FACT DC>8826 are designed LU-proof
LIN	P54PCT245	Logic	CMOS	PFS	–	<27	–	BNL	4/91
A	25HCT04	SAR	CMOS	ZYR	–	22	3E-4	88-In	7/91

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